Energy Efficient Embedded Non-Volatile Memory & Logic Based on Ferroelectric $Hf(Zr)O_2$

3eFERRO develops a competitive scalable FeRAM and logic-in-memory designs based on Si-compatible ferroelectric $Hf(Zr)O_2$ to improve energy efficiency of IoT. The project gathers expertise from France, Germany, Romania, Switzerland, and Greece, to face challenges in materials, circuit design and integration with Si CMOS.

At A Glance: 3eFERRO

Energy Efficient Embedded Non-Volatile Memory and Logic Based on Ferroelectric $Hf(Zr)O_2$.

Project Coordinator

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Partners: *ST Microelectronics (FR), NaMLab (DE), NIMP (RO), EPFL (CH), ECL (FR), NCSRD (EL), FZJ (DE)*

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EC Contribution: *€* **3.99***m*

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Main Objectives

The 3eFERRO consortium seeks for energy efficient non-volatile memory (NVM) and logic devices based on Si-compatible ferroelectric (FE) HfO_2 to provide advanced embedded solutions for normally-off microcontroller units (MCU) used in IoT. The consortium is a balanced mix of integrated device manufacturer (IDM), large technology development laboratories, and academia to face complex issues associated with materials research and development, circuit design, device fabrication and integration of novel FeRAM with Si CMOS

Long Term Impact on Nanoelectronics and IoT

One of our long term goals is to replace flash NVM in normally-off MCUs with faster and less power consuming ferroelectric NVM and combine it with novel logic-in-memory (LiM) designs in order to enhance their energy efficiency to face the challenges of edge computing in IoT. Equally important is our goal to support LiM with steep slope switching boosters that will further enhance low power operation without compromising performance. Our main strategy to achieve our goals is to introduce Si-compatible FE HfO_2 which will allow achieving a competitive FeRAM with good prospects for manufacturability and cell size scaling. FE HfO_2 is also expected to enable negative capacitance field effect transistors operating as low power steep slope switches.

3eFERRO is the only project about ferroelectric memories in H2020-ICT

What Can We Learn from 3eFERRO?

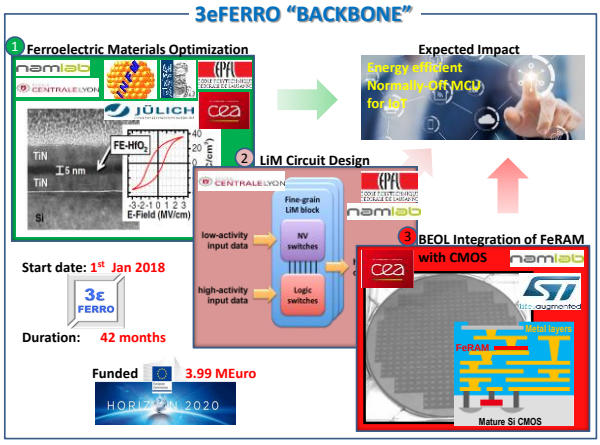
Introducing new materials and device architectures often creates a lot of unknowns. In 3eFERRO we will learn what it takes to make a competitive FE-HfO_2 –based FeRAM that will retain the merits of conventional perovskite-based FeRAM and overcome their shortcomings providing better manufacturabilty and scalability. Moreover, we expect to learn whether the FE HfO_2-based FeRAM offers performance advantages compared to other NVM rivals. One of the big unknowns is whether FE HfO2 based memory will be able to meet the high endurance requirements. It is also not known whether ferroelectricity in this material can be achieved at low temperatures that will allow BEOL integration of 1T-1C arrays with CMOS. Moreover, we expect to learn about interface engineering methodologies that could improve endurance of FeFET devices

Technical Approach

The project has three core tasks that can be considered as the 3eFERRO "backbone"

1. **Optimization of FE Hf(Zr)O_2 materials.** Led by NaMLab, emphasis is given on the compatibility with Si processing. ALD and various PVD growth methodologies will be used as well as advanced structural physical and electrical characterization techniques to determine the factors limiting reliability of ferroelectric capacitors
2. **LiM circuit design.** Led by ECL, fine-grain LiM designs will be developed with low power/ high performance NCFET booster tech-nologies. PDK kit will be developed and circuit fabrication will be outsourced to external foundries to produce MPW chips using already developed HfO_2 FeFET technologies.
3. **Back-end of line integration with Si CMOS.** The MAD 200 mm pilot line of CEA-Leti will be used to fabricate 1kbit FeRAM arrays of 1C-1T capacitors on the BEOL of mature Si CMOS and benchmark with other RAM technologies

All core tasks and the participants' involvement are illustrated in the figure below.



For efficient implementation, the workplan is structured in six workpackages (WP): WP1-Projet Decision Making & Management; WP2-Development and Optimization of FE materials for Memory Applications; WP3-FE Behaviour Through Advanced Characterization; WP4-New Concepts and Designs for Energy-Efficient Embedded FE Computing; WP5-Demonstration and Evaluation of FE NVM Arrays and LiM Circuits based on Optimized Materials and Advanced Designs; WP6-Dissemination, Communication, Exploitation, and Training Activities

Key Issues/Challenges

The main technical challenges are summarized below:

- **Improve the endurance of HfO_2 FeRAM and FeFETs**. Improve the ferroelectric-electrode interfaces by introducing suitable dopant materials to overcome fatigue and extend the endurance from ~10^{10} which is today to essentially unlimited endurance (>10^{15} cycles) obtained from the conventional (but not scalable) perovskite-based FeRAM.
- **Mitigate the wake-up and imprint effects**. These two effects are related and limit the applicability of FE HfO2 in memory applications. A difficult challenge is to improve wake-up effects without compromising endurance at large cycling number regime
- **Develop low temperature processing of FeRAM to enable BEOL integration with CMOS**. The main target will be to reduce the crystallization /FE phase formation temperature below 400-450 ^{o}C to allow BEOL integration with CMOS, without compromising performance characteristics (i.e remnant polarization, coercive field) and reliability. Avoiding cross contamination due to introduction of new (dopant) materials in an advanced Si pilot line could be challenging.
- **Develop appropriate ferroelectric/dielectric gate stacks for NCFETs.** The realization of well-controlled FE NCFET technology remains elusive since it was first proposed in 2008. The identification of appropriate ferroelectric/ normal dielectric combination to obtain a steep slope (SS< 60 mV/dec) switch with a stable low voltage operation is challenging.

Expected Impact

The project output is expected to surpass the technical objectives and have a wider and deeper impact. First, it is expected that it will satisfy the urgent needs of European integrated device manufacturers and microelectronic key industry, and help them establish their leading position in the IoT market with substantially improved or innovative MCU component products. Second, it will place European stake holders in the "pole position" in the race for a universal memory which will combine the benefits of a high storage density medium (typically found in solid state drivers) with the high speed of SRAM. This could bridge the gap in performance between processors and memories and help the future development of data-centric computation systems where advanced memories with processing capabilities can play a critical role.