Energy Efficient Embedded Non-Volatile Memory & Logic Based on Ferroelectric $Hf(Zr)O_2$

3εFERRO focuses on competitive, scalable FeRAM and logic-in-memory based on Si-compatible, ferroelectric $Hf_xZr_{1-x}O_2$. We report interface engineering, capacitor integration, FeFET and FeRAM logic design.

Energy efficiency

The 3εFERRO consortium is researching energy efficient non-volatile memory and logic devices based on Si-compatible ferroelectric $HfZrO_2$ (HZO) to provide advanced embedded solutions for normally-off microcontroller units used in IoT. The consortium is a balanced mix of large technology development laboratories and academia in partnership with ST Microelectronics to address the complex issues associated with materials optimization, circuit design, device fabrication and integration.

At A Glance

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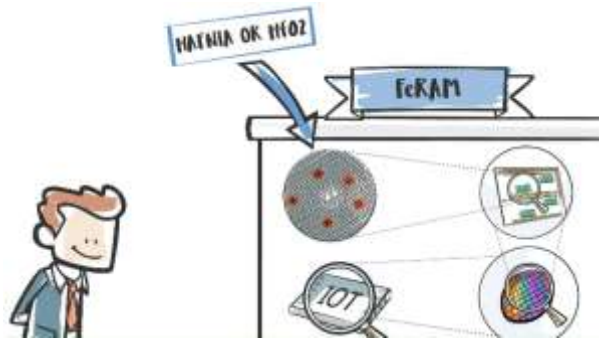
Duration: 01/01/2018 – 30/06/2021

Funding scheme: RIA
EC Contribution: € **3.99**m

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 780302

Video 3εFERRO now available

The 3εFERRO partners have commissioned the Minimento company ((www.minimento.fr), to realize a video presentation of the project suitable for distribution to a wide audience.



The video will hopefully be an attractive introduction to the project work and the broader scientific context. It can be viewed here:

https://www.youtube.com/watch?v=M8tL-nN7G-A

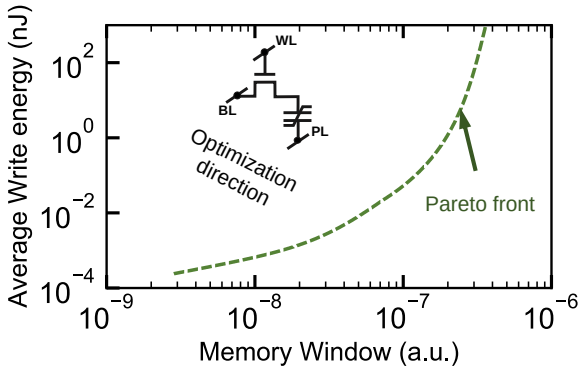
Exploration of the Design Space of ferroelectric-based circuits through a Design-Technology co-optimization approach

Exploring the full possibilities offered by FeRAM or FeFET for eNVM or Logic in Memory (LiM) architectures in a cost-effective manner, and projecting device characteristics onto meaningful system-level performance metrics, requires going beyond the current performance levels of hardware, both in terms of device characteristics and hardware complexity.

In a simulation-oriented approach, a scalable benchmarking platform has been set up by ECL-INL for use in both 1T-1C and FeFET-based design space exploration. This targets a methodological

design-technology co-optimization approach (DTCO) in order to bridge the gap between device-level performance characteristics and system-level performance metrics while considering architectural specificities.

Here, the objective is to apply multi-objective optimization algorithms to simulation-based evaluation of ferroelectric device-based circuits (such as a1T-1C memory cell based on FeRAM devices, or a NV-NAND gate based on FeFET devices).



The simulation is based on standard EDA design tools and relevant technology PDKs, as well as the ferroelectric capacitance compact model developed in Verilog-A by NamLab, while the optimization platform is based on an existing multi-domain synthesis tool developed by ECL-INL. The outcome of this step is data and mathematical models expressing tradeoffs between performance metrics (in the form of *Pareto Fronts*) and associated design data (*Pareto Sets*). This data can then be used in system-level performance evaluation and benchmarking by exploiting architectural models in order to quantify relevant metrics such as configuration / runtime energy and latency, complexity or accuracy.

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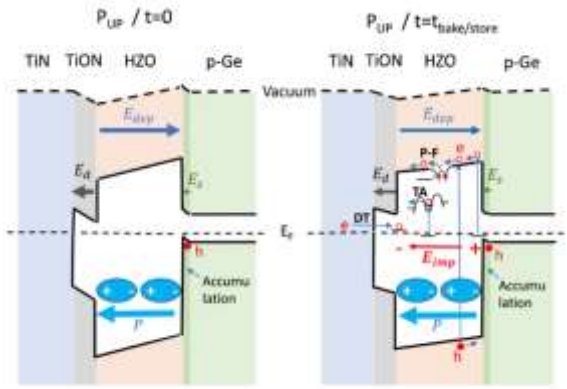
Imprint in TiN/HfZrO$_2$/Ge capacitor structures

Imprint is one of the main reliability concerns of ferroelectric HZO resulting in retention loss and read errors in ferroelectric nonvolatile memories. Information can be stored in one of the two stable polarization states. Then, imprint manifests itself as an increase over time of the coercive voltage for switching to the opposite state. NCSRD "Demokritos" institute in Athens has provided a comprehensive study of the imprint effects in Ge MFS capacitors with ferroelectric HZO fabricated by plasma assisted atomic oxygen deposition.

Our results show that the imprint is dominated by carrier injection at the top TiN/HZO interface. In short, direct tunneling through the potential barrier of the interfacial dielectric (dead) layer allows exchange of carriers between the metallic electrodes and oxygen vacancy defects at the interfaces. The injected carriers establish an imprint field in the direction of polarization thus stabilizing the stored polarization state and, consequently, increasing the voltage that is needed to switch to the opposite state.



The reduced imprint observed in our devices is attributed partly to the clean Ge/HZO interfaces which are unique for Ge when used as bottom electrode. It is also found that reliability effects such as imprint and endurance depend sensitively on the type of the crystallization annealing that is used. Details can be found in C. Zacharaki et al., "Reliability aspects of ferroelectric TiN/$Hf_{0.5}Zr_{0.5}O_2$/Ge capacitors grown by plasma assisted atomic oxygen deposition" *Appl. Phys. Lett*. **117**, 212905 (2020) 2020; https://doi.org/10.1063/5.0029657

High k workshop virtual seminars programme

Given the ongoing crisis due to the Covid-19, the traditional high k workshop organized in the springtime by 3εFERRO partner NaMLab will not take place as planned. Instead, NaMLab and 3εFERRO have organized a series of virtual seminars on all aspects of hafnia-based ferroelectrics. International guest speakers including Beatriz Noheda, Alexei Gruverman, Alfred Kersch, Sayeef Salahuddin, Min Hyuk Park, Anna Chernikova and Ulrich Boettger will join 3εFERRO scientists to present topics covering film synthesis, advanced characterization, circuit design and modelling to processing.

Six weekly sessions with three presentations per session will be organized in April-May 2021. The series is open to all, online registration will be possible one month before the start of the sessions through the NaMLab website here:

http://namlab.de/high-k-workshop-2021-virtual